SPECIFICATION

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[STI METHOD FOR SEMICONDUCTOR PROCESSES]

Background of Invention

[0001] 1. Field of the Invention

[0002] The present invention relates to a shallow trench isolation (STI) method, and more particularly, to a shallow trench isolation method utilizing a high temperature oxide (HTO) film that functions as an interface reinforcement layer to protect a shallow trench edge.

[0003] 2. Background of the Invention

[0004] Usually applied to semiconductor components, local oxidation of silicon (LOCOS) technology used in a conventional VLSI front end has become inefficient. Bird's beak effects in LOCOS technology has resulted in LOCOS technology not being used in high precision wafer processing. Instead, LOCOS structures have been replaced by shallow trench isolation (STI) structures, which are another form of component isolation technology. In accordance with advancements in defect detecting engineering, STI component isolation technology is found to suffer from random bit failures, which leads to an increase of current leakage in components, and decay of the STI structure. The reliability of the resulting product is thus affected.

[0005] Please refer to Fig.1 to Fig.7 of diagrams of a prior shallow trench isolation (STI) method. As shown in Fig.1, the prior art utilizes a substrate 101 to etch a trench region 102. The method to form the trench region 102 uses a mask layer 106 above a top surface of the substrate 101. The mask layer 106 is employed to define a location of the trench region 102. A dry-etching process (such as a reactive ion etching process) is then performed to etch the substrate so as to form the trench region 102.

The mask layer 106 is a stacked layer, which comprises a pad oxide layer 103, a silicon nitride layer 104, and a dielectric anti-reflection coating (DARC) layer 105. SiON is generally used to form the DARC layer 105. Conventional photolithography processes and etching processes are used to define the mask layer 106.

[0006] As shown in Fig.2, a thermal oxidization process utilizes oxygen functioning as a reaction gas, at a temperature of 900 ° C, to form a pad layer 107 with a thickness of 200 angstroms oxidized on a top surface of the substrate 101 within the trench region 102. The major objective in forming the pad layer 107 is to reverse lattice destruction of the substrate 101 that occurs when performing a dry-etching process to form the trench region 102. Then, a high-density plasma chemical vapor deposition (HDPCVD) process deposits an HDP oxide layer 108 to cover the mask layer 106, and fill the trench region 102.

[0007] As shown in Fig.3, a photoresistor layer 110, also called a reverse HDP oxide mask, covers the trench region 102, and a HDP oxide layer etching process etches the HDP oxide layer 108 outside the trench region 102. The major objective of the reverse HDP oxide mask and the HDP oxide layer etching process is to prevent subsequent chemical mechanical polishing (CMP) from causing a dishing effect in the trench region 102. After stripping the photoresistor layer 110, as shown in Fig.4, a CMP process planarizes the HDP oxide layer 108. At the end of the CMP process, the CMP process is stopped on the surface of the silicon nitride layer 104, and a remaining thickness of the silicon nitride layer 104 is left at 1300 angstroms.

[0008] As shown in Fig.5, a STI corner rounding process utilizing a wet oxidation method, at a high temperature of 1075 ° C, oxidizes the substrate 101 of a STI corner region 114. As shown in Fig.6, then an acid solution dipping process utilizes a diluted HF (DHF) solution (50:1) to clean the surface of the substrate 101 in a few minutes at room temperature, so as to remove the residual silicon oxide from the silicon nitride layer 104 and simultaneously etch the HDP oxide layer 108 to a predetermined thickness within the trench region 102.

[0009] Generally, a height of the HDP oxide layer 108 within the trench region 102 is not high enough to allow etching of the HDP oxide layer 108 for a few hundred angstroms. Unfortunately, the diluted HF (DHF) solution corrodes the HDP oxide layer

108 of the STI corner region 114 to form small voids, also called edge voids 116. This occurs because a surface binding force between the HDP oxide layer 108 and the silicon nitride layer 104 is not strong enough to resist acid solution corrosion, so producing a phenomenon of acid penetration.

[0010] As shown in Fig.7, a thermal phosphoric acid solution is used to clean the silicon nitride layer 104. Then, a diluted HF (DHF) solution (100:1) cleans the surface of the substrate 101 in few minutes at room temperature. The previous edge voids 116 cause the acid solution to accumulate, and corrode the HDP oxide layer 108 along the edge voids 116 to form a seam defect 118. The seam defect 118 seriously affects the isolation effect of the STI, and increases current leakage.

[0011] The prior art STI method needs to repeat the acid solution dipping process a number of times in order to achieve the objectives of cleaning the surface and stripping the silicon oxide layer, affected by the acid solution corrosion. Furthermore, the oxide layer forming process, also requires the diluted HF (DHF) solution to be employed many times so enhancing the acid penetration phenomenon"s effect. The edge voids 116 and the seam defect 118 are randomly formed, so the STI method is very difficult to improve by performing extra remedial measures. Additionally, the edge voids 116 and the seam defect 118 causes abnormality in the electrical conductivity of semiconductor components. This abnormality can be seen in a double hump variation of the Id/Vg curve.

Summary of Invention

[0012] It is therefore a primary objective of the present invention to provide a shallow trench isolation method utilizing a high temperature oxide (HTO) film to function as an interface reinforcement layer to protect a shallow trench edge, and thus effectively avoid an acid corroded seams problem.

[0013] The present invention discloses a shallow trench isolation (STI) method for use in semiconductor processes. This method comprises, providing a substrate with a top surface, and forming a trench-patterned mask layer on the top surface to expose an unmasked trench region of the substrate, the mask layer includes a pad oxide layer and a silicon nitride layer formed on the pad oxide layer. The unmasked region of the

substrate is etched to form a trench in the substrate. A HTO (high temperature oxide) film is deposited over the substrate to cover the trench and the mask layer. A dielectric layer fills the trench and covers the HTO film. The dielectric layer is planarized to expose the silicon nitride layer and then the silicon nitride is stripped. Thereafter at least one acid solution dipping process is performed.

[0014] It is an advantage of the present invention that a high temperature oxide (HOT) film is used to avoid acid corroded seams problem and production of shallow trench seams defects.

[0015] These and other objectives and advantages of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

[0016] Fig. 1 to Fig. 7 are diagrams of a prior art shallow trench isolation (STI) method; and Fig. 8 to Fig. 14 are diagrams of a shallow trench isolation (STI) method according to the present invention

Detailed Description

[0017] Please refer to Fig. 8 to Fig. 14 of diagrams of a shallow trench isolation (STI) method according to the present invention. As shown in Fig. 8, a silicon substrate 201 is provided. In the optimal preferred embodiment, the silicon substrate 201 is a P-type doped single crystal silicon substrate with a crystal direction <100>. Nevertheless, the silicon substrate 201 can also be a silicon-on-insulator (SOI) substrate, an epitaxy silicon substrate or another silicon substrate with a different crystal structure. Then, a pad oxide layer 203 with a thickness between 100 to 300 angstroms is formed on the surface of the silicon substrate by thermal oxidization, at a temperature of 900 ° C and in an oxygen/hydrogen environment. An optimal thickness of the pad oxide layer 203 is 200 angstroms.

[0018] Using a chemical vapor deposition (CVD) method, such as a low pressure chemical vapor deposition (LPCVD), a silicon nitride layer 204 with a thickness between 1800 and 2000 angstroms is deposited on the pad oxide layer. The silicon nitride layer 204

is formed, using dichlorosilane (SiH_2Cl_2) and ammonia as reaction gases, at a pressure of 0.3 Torr and a temperature of 750 ° C. The silicon nitride layer 204 is coated with an anti-reflection layer, that is also called a dielectric anti-reflection coating (DARC) layer 205. The DARC layer 205 is composed of SiON, with a thickness of 500 angstroms. A stacked mask 206 comprises the pad oxide layer 203, the silicon nitride layer 204 and the DARC layer 205, defining a trench isolation region.

[0019] As shown in Fig. 8, a photolithography process and an etching process are used to etch the surface of the silicon substrate 201 to form a trench region 202. The method of forming the trench region 202 uses the stacked mask 206 to define a location of the trench region 202 on the silicon substrate 201, and following that a dry-etching process (such as REI process) etches the silicon substrate 201 in order to form the trench region 202. With the trench region 202 formed the thickness of the silicon nitride layer 204 remains 1700 angstroms.

[0020] As shown in Fig. 9, an LPCVD process is performed to deposit a high temperature oxide (HTO) film 207, with a thickness of 200 angstroms, on the surface of the silicon substrate 201. The HTO film 207 covers the surface of the silicon substrate 201 and the surface of the stacked mask layer 206. Another method of forming the HTO film 207 uses dichlorosilane and nitrous oxide (N_2O) to function as reaction gases, at a pressure of 0.4 Torr and at a reaction temperature of 700 ° C~850 ° C (optimal temperature is 780 ° C). The flow rate of dichlorosilane is 0.12~0.18 standard liters per minute (SLM), with an optimal flow rate of 0.15 SLM. The flow rate of N_2O is 0.2~0.35 SLM, with an optimal flow rate of 0.3 SLM. Then, the HDPCVD process is performed to deposit a HDP oxide layer 208, with a thickness of 8000 angstroms, to fill the trench region 202 containing the HTO film 207.

[0021] As shown in Fig. 10, a photoresistor layer 210, also called a reverse HDP oxide mask, is used to cover the trench region 202, and a HDP oxide layer etching process etches the HDP oxide layer 208 outside the trench region 202. The major objective of the reverse HDP oxide mask and the HDP oxide layer etching process is to avoid the proceeding chemical mechanical polishing (CMP) process causing a dishing effect in the trench region 202. After stripping the photoresistor layer 210, as shown in Fig. 11, a CMP process planarizes the HDP oxide layer 208. The CMP process is not

performed on the surface of the silicon nitride layer 204. A remaining thickness of the silicon nitride layer 204 is left at 1200~1300 angstroms. When the CMP process is finished, the present invention HTO film 207 protects an interface between the HDP oxide layer 208 and the silicon nitride layer 204. The HDP film 207 and the silicon nitride layer 204 are tightly combined to prevent acid penetration, and further, to protect the interface between the HDP oxide layer 208 and the silicon substrate 201 so as not to produce the prior art STI seam defects.

[0022] As shown in Fig. 12, then a STI corner rounding process utilizes a wet oxidation method, under a high temperature of 1075 ° C, to oxidize the substrate 201 of a STI corner region 214. As shown in Fig. 13, a silicon oxide dry-etching process is then performed to etch the residual silicon oxide on the silicon nitride layer 204 and to simultaneously etch the HDP oxide layer 208 with a predetermined thickness within the trench region 202. The major objective in performing the dry-etching process is to achieve the conventional acid solution dipping process and further reduce the probability of acid penetration.

[0023] Nevertheless, in the other preferred embodiments of the present invention, the conventional acid solution dipping process can also be used. Diluted HF (DHF) solution (50:1) is used to clean the surface of the substrate 201 in few minutes, at room temperature, so as to remove the residual silicon oxide on the silicon nitride layer 204 and to simultaneously etch the HDP oxide layer 208 with a predetermined thickness within the trench region 202. The binding force between the HTO film 207, the silicon nitride layer 204 and the HDP oxide layer 208 is stronger, so that acid penetration does not occur.

[0024] As shown in Fig. 14, thermal phosphoric acid solution heated to a temperature of 160 ° C is used to strip the silicon nitride layer 204. Then, diluted HF solution (100:1) cleans the surface of the substrate 201 in few minutes at room temperature. The present invention has an obvious effect of stopping acid penetration from causing the STI seam defects. The HTO film 207 functioning as an interface reinforcement layer enables the silicon nitride layer 204 and the HDP oxide layer 208 to tightly combine so as to choke the acid penetration passage.

[0025] In contrast to the prior art, the present invention has following characteristics:(1)

utilizing the HTO film 207 to replace the prior art pad layer formed by a thermal oxidization process, avoiding an acid corroded seams problem that produces the STI seam defects;(2)the HTO film 207 defined as a chemical vapor deposition film, having a higher conformity than the prior art pad layer formed by the thermal oxidization process and so preventing STI holes occurring; and(3)utilizing the compact nature of the HTO film 207 to protect the STI corner region 214.

[0026] Those skilled in the art will readily observe that numerous modification and alterations of the advice may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.